IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Terrence C. Leslie	Examiner:	Matthew C. Landau
Serial No.:	10/765,301	Group Art Unit:	2815
Filed:	January 27, 2004	Docket:	303.860US1
Title:	SELECTIVE EPITAXY VERTICAL INTEGRATED CIRCUIT COMPONENTS AND METHODS		

SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT

MS Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

In compliance with the duty imposed by 37 C.F.R. § 1.56, and in accordance with 37 C.F.R. §§ 1.97 *et. seq.*, the enclosed materials are brought to the attention of the Examiner for consideration in connection with the above-identified patent application. Applicant respectfully requests that this Supplemental Information Disclosure Statement be entered and the documents listed on the attached Form 1449 be considered by the Examiner and made of record. Pursuant to the provisions of MPEP 609, Applicant requests that a copy of the 1449 form, initialed as being considered by the Examiner, be returned to the Applicant with the next official communication.

Pursuant to 37 C.F.R. §1.97(c)(2), Applicants hereby authorize the Commissoner to charge the fee of $180.00 as set forth in 37 C.F.R. §1.17(p), to Deposit Account No. 19-0743. Please charge any additional fees or credit any overpayment to Deposit Account No. 19-0743.

The Examiner is invited to contact the Applicant's Representative at the below-listed telephone number if there are any questions regarding this communication.

Pursuant to 37 C.F.R. 1.98(a)(2), Applicant believes that copies of cited U.S. Patents and Published Applications are no longer required to be provided to the Office. Notification of this change was provided in the United States Patent and Trademark Office OG Notices dated October 12, 2004. Thus, Applicant has not included copies of any US Patents or Published Applications cited with this submission. Should the Office require copies to be provided, Applicant respectfully requests that notice of such requirement be directed to Applicant's below-signed representative. Applicant acknowledges the requirement to submit copies of foreign patent documents and non-patent literature in accordance with 37 C.F.R. 1.98(a)(2).

Respectfully submitted,

TERRENCE C. LESLIE

By his Representatives,

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Date 4 May '06

By
Timothy B Clise
Reg. No. 40,957

CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being filed using the USPTO's electronic filing system EFS-Web, and is addressed to: Commissioner for Patents, P O Box 1450, Alexandria, VA 22313-1450, on this 5th day of May, 2006.

5th May 2006

JUDY DETN
Name

Signature

PTO/SB/08A(10-01)
Approved for use through 10/31/2002 OMB 651-0031
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Substitute for form 1449A/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

Complete if Known	
Application Number	10/765,301
Filing Date	January 27, 2004
First Named Inventor	Leslie, Terrence
Group Art Unit	2815
Examiner Name	Landau, Matthew
Sheet 1 of 1	Attorney Docket No: 303.860US1

US PATENT DOCUMENTS				
Examiner Initial*	**USP Document Number**	**Publication Date**	**Name of Patentee or Applicant of cited Document**	**Filing Date If Appropriate**
	US-6,687,146	02/03/2004	Kurjanowicz, Wlodek , et al.	01/31/2002

FOREIGN PATENT DOCUMENTS				
Examiner Initials*	**Foreign Document No**	**Publication Date**	**Name of Patentee or Applicant of cited Document**	**T²**

OTHER DOCUMENTS -- NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	**Cite No [1]**	**Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.**	**T²**
		DEFFREE, SUSAN , "IBM proves vertical transistor DRAM at 70nm", Electronic News, (June 10, 2003),2 pgs	
		HERGENROTHER, J M., et al., "The vertical replacement-gate (VRG) MOSFET: a 50-nm vertical MOSFET with lithography-independent gate length", Bell Laboratories, Lucent Technologies, Murray Hill, 4pgs	
		ISA, "IBM claims speediest silicon transistor", http://www.isa.org/Template.cfm?Section=Communities&template=/TaggedPage/DetailDisplay.cfm&ContentID=20445, ISA - The Instrumentation, Systems and Automation Society,(November 4, 2002),2 pgs	
		LUCENT TECHNOLOGIES, "Revolutionary transistor design turns the silicon world on end", http://www.bell-labs.com/news/1999/november/15/1.html, Lucent Technologies, Bell Labs Innovations,(1999),3 pgs	
		LUCENT TECHNOLOGIES, "Revolutionary transistor turns silicon world on end", (2000),2 pgs	
		NING, T H., "Why BiCMOS and SOI BiCMoS?", IBM, 0018-8648,(11.29.01),7 pgs	

EXAMINER **DATE CONSIDERED**

* EXAMINER: Initial if reference considered whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. 1 Applicant's unique citation designation number (optional) 2 Applicant is to place a check mark here if English language Translation is attached